Analysis of Electrostatic Discharge (ESD) for 3DIC systems

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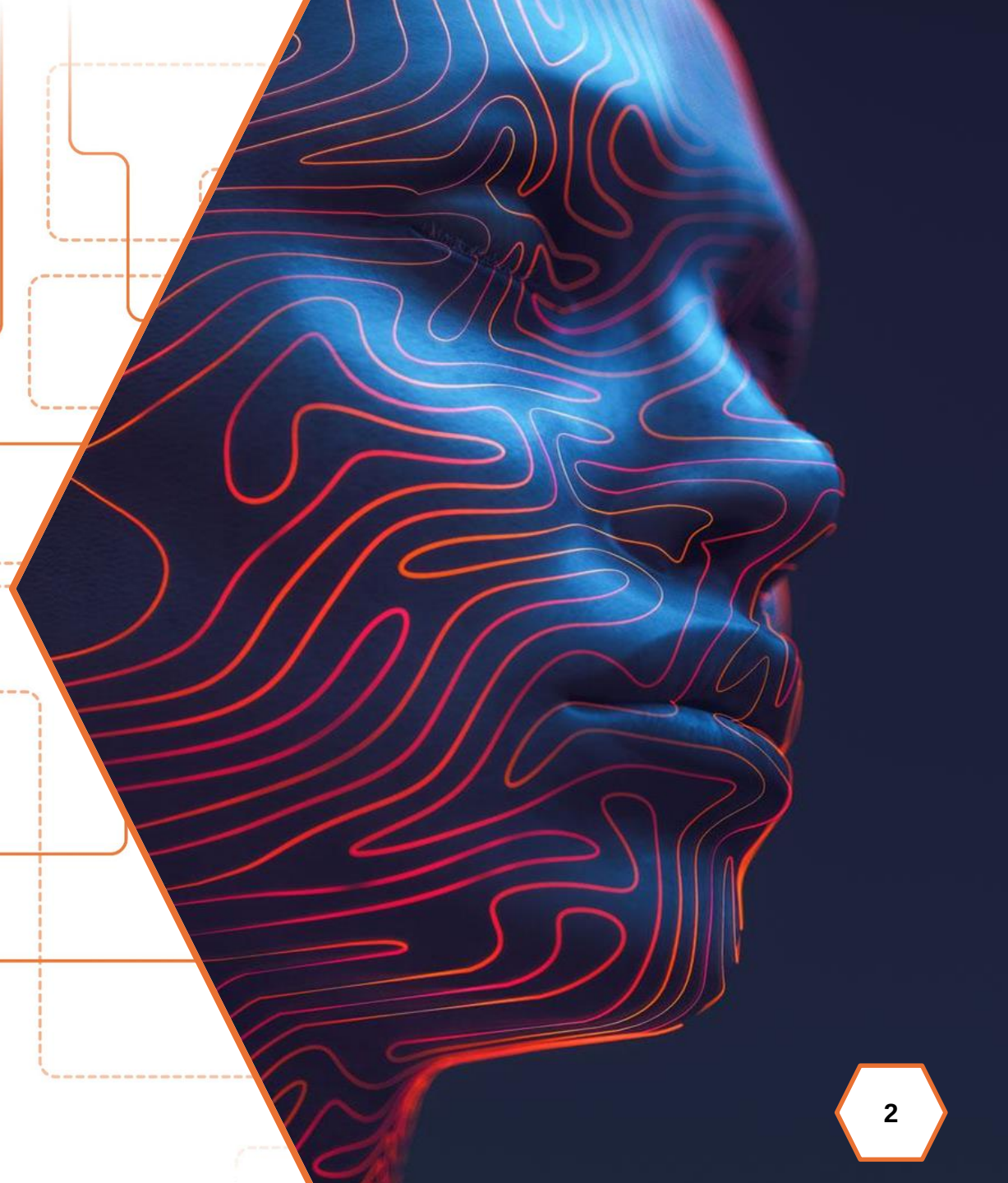
Background

- Multi-die (2.5D and 3D) systems present new challenges in their potential vulnerability to Electrostatic Discharge (ESD) events.
- Traditional ESD sign-off analysis involves assessing the vulnerability of circuitry and on-chip routing to zap events that occur within a single die
  - Now with multi-die systems, discharge paths for electrostatic charge can occur from die-to-die.
- The potential discharge paths from one die to another and the impact of these discharge paths need to be assessed through simulation
  - →to properly deem the multi-die system (often involving unique interposer/integrated packaging technologies as well) safe for production



Main Idea/purpose

- Demonstrate that it’s possible to perform ESD checks for multi-die 3DIC systems and to visualize the results. Prior methods involved standalone die analyses.
- Identify potential differences in violations on a particular die in a multi-die ESD analysis that would otherwise be very difficult or impossible to uncover in a standalone analysis of the same die

- Assessment Methodology:
  - Apply well-established ESD simulation methodology to the entire multi-die system.
  - Include paths from die-to-die and package side bumps.
  - Use novel simulation tools for comprehensive analysis.

- Simulation Checks:
  - Run Current Density (CD) checks and Resistance (R) checks against technology-specific rules.
  - Allow zap currents to traverse from die-to-die.
  - Apply the same CD and R checks used for single-die designs.

- Modeling Capabilities:
  - Stitch two different dies together for simulation.
  - Simulate current flow during zap events along various potential paths.
  - Discover potential differences in violations on a given die within a combined system.

Single Die vs Multi Die ESD checks

The below is a simplified illustration of why it's important to **assess the 3DIC system for ESD vulnerability** (vs single die assessed independently)

- The **ESD discharge path extends across multiple die** and must be accounted for to accurately assess resistive paths that traverse the multiple die. The drawing is a simplification of the thousands of hybrid bonds that exist, and complexity of the R network would increase with the presence of a bridge/interposer. A manual effort to perform P2P Res checks would be impractical.

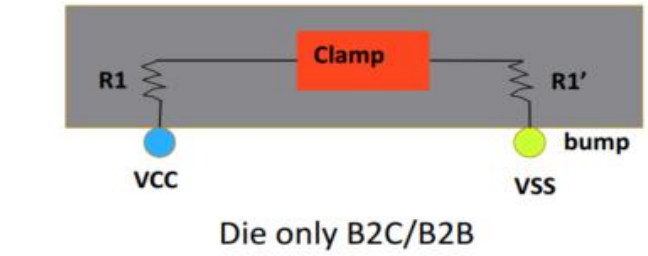
Point-to-Point (P2P) Resistance Check: **3DIC Configuration Shows Higher Bump-to-Clamp (B2C) resistance**

- Both Single Die and 3DIC runs have 1 path from bump to clamp
- There is no Parallel Path, so series resistances are added in 3DIC

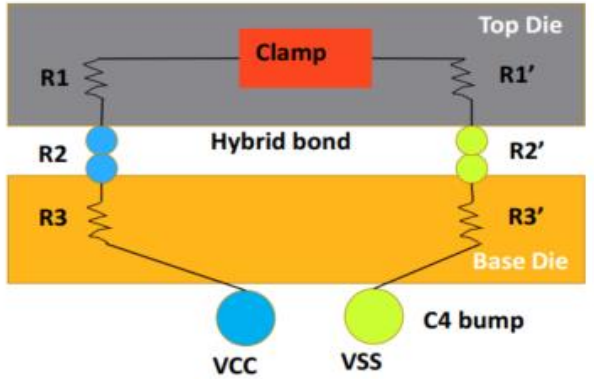
	Die Only	3DIC
B2C	R1 or R1'	R1+R2+R3 Or R1'+R2'+R3'
B2B	R1 + R1'	(R1+R2+R3) + (R1'+R2'+R3')

3DIC Run show increased resistance

	Die Only		3DIC	
	Min	Max	Min	Max
B2C	0.0097	0.0099	0.0121	0.0165
B2B	0.0239		0.0265	

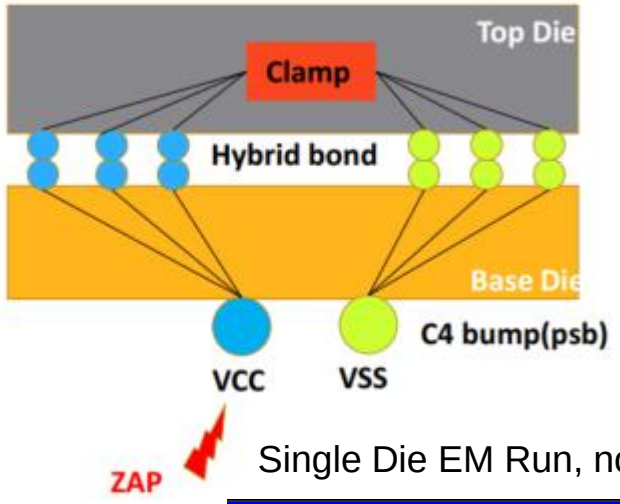


Die only B2C/B2B



3DIC B2C/B2b

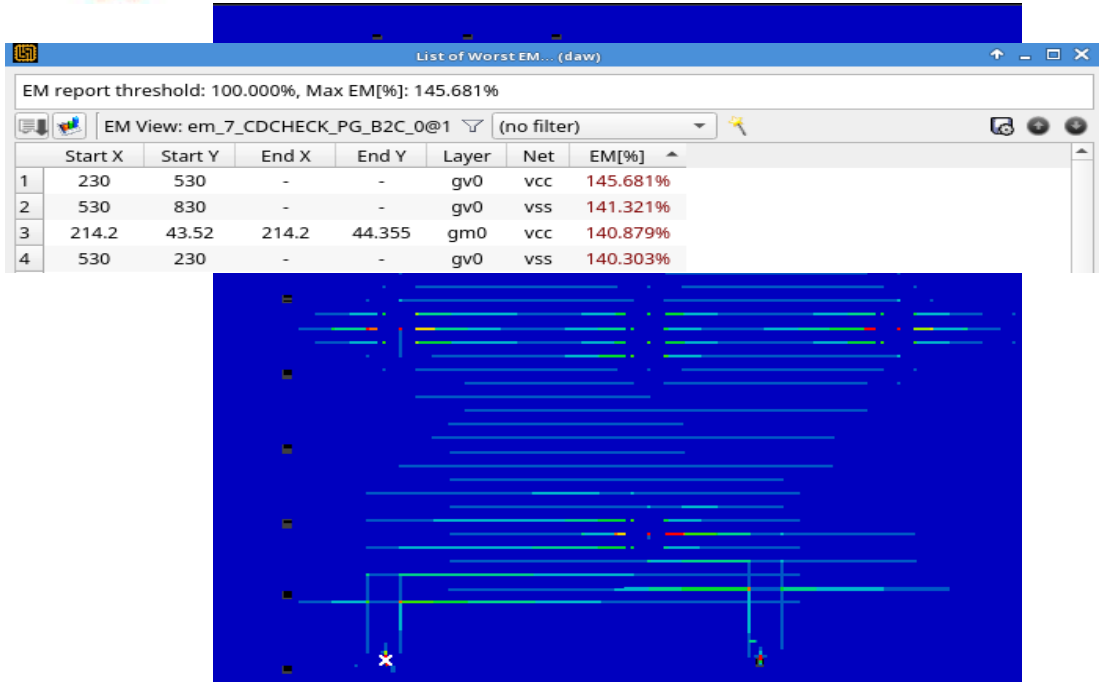
Electromigration (EM) can change when performing single die VS multi-die analysis



- Deltas in current distribution occur when accounting for the cumulative R network of combined stitched die
- Single Base die (left) shows more visible lateral current vs Base die in multi die configuration (right) since the 3DIC configuration introduces for more vertical Power and Ground current paths through hybrid bonds (HB)

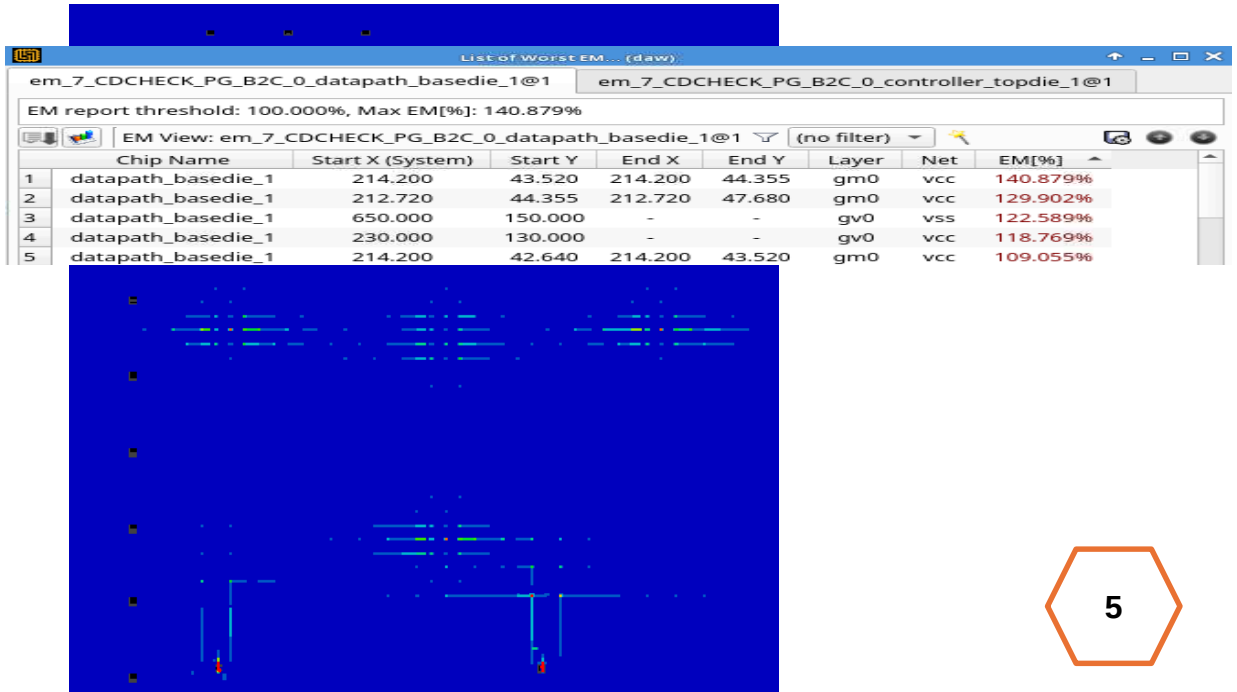
- Top and Base die have 5 clamp cells and we Zap current on Package side bump
- Top and Base dies are connected by more than 15K HBs
- Current Flows from C4 to base die, then though HB to Top Die

Single Die EM Run, no HBs (Base Die only)



	Start X	Start Y	End X	End Y	Layer	Net	EM[%]
1	230	530	-	-	gv0	vcc	145.681%
2	530	830	-	-	gv0	vss	141.321%
3	214.2	43.52	214.2	44.355	gm0	vcc	140.879%
4	530	230	-	-	gv0	vss	140.303%

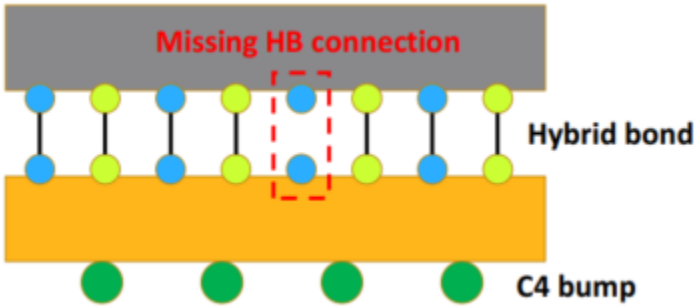
3DIC EM Run (Base Die shown, with Top Die Attached but not shown)



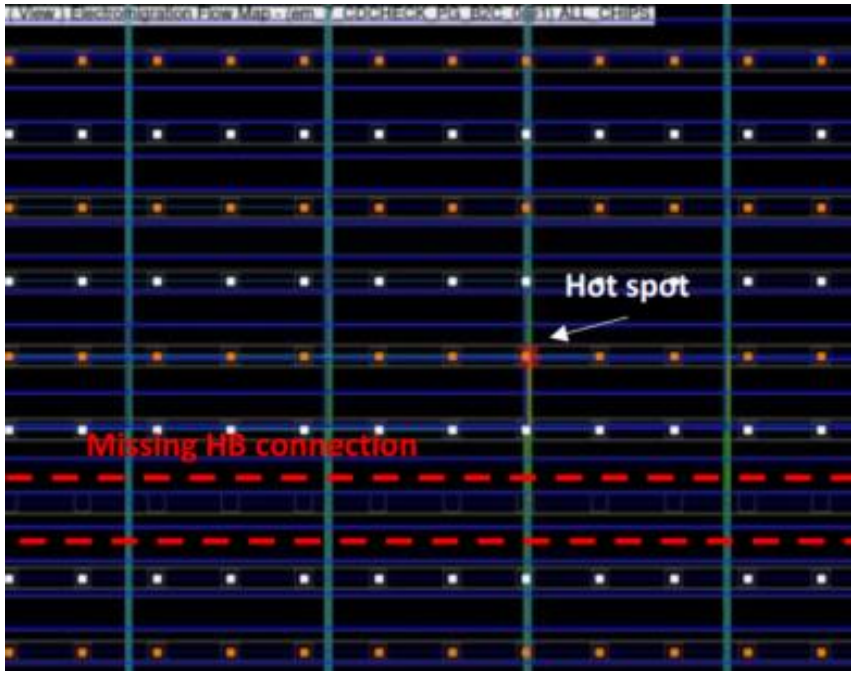
	Chip Name	Start X (System)	Start Y	End X	End Y	Layer	Net	EM[%]
1	datapath_basedie_1	214.200	43.520	214.200	44.355	gm0	vcc	140.879%
2	datapath_basedie_1	212.720	44.355	212.720	47.680	gm0	vcc	129.902%
3	datapath_basedie_1	650.000	150.000	-	-	gv0	vss	122.589%
4	datapath_basedie_1	230.000	130.000	-	-	gv0	vcc	118.769%
5	datapath_basedie_1	214.200	42.640	214.200	43.520	gm0	vcc	109.055%

3DIC (multi-die) run can help find connectivity issues between two die

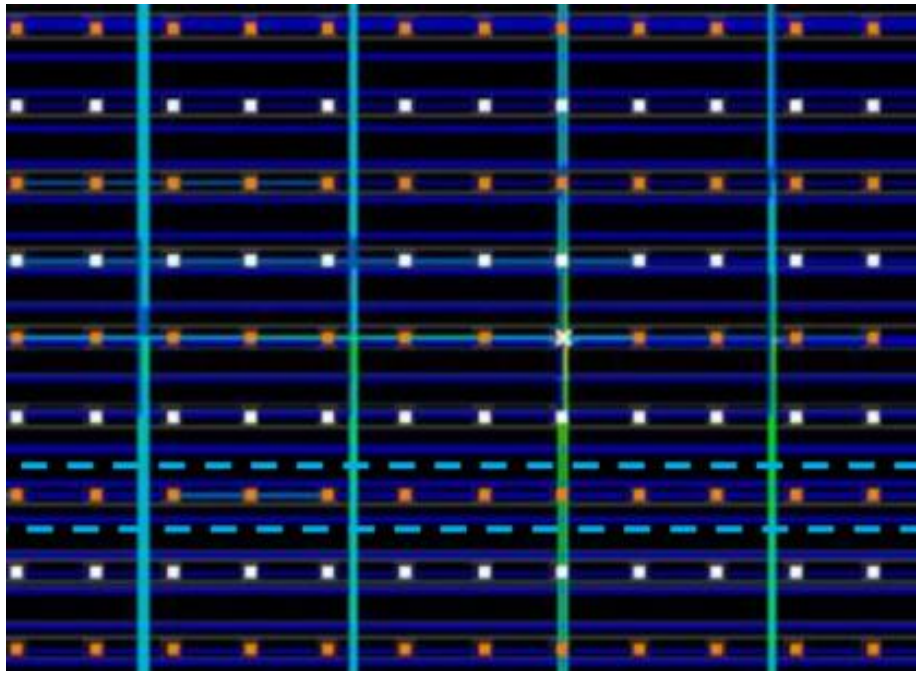
- 3DIC run led to a **discovery of missing HB connections** in the region, resulting in EM violations (lower left image)
- **Correcting these missing HBs resolves the EM hotspot** (lower right image)
- This type of multi-die analysis can also serve as a way to do early floorplanning by experimenting with hybrid bonding density that satisfies EM
- Fixing HB connection eliminated the EM hotspot
- The EM hotspot was on a layer below HB and current passed through this layer to Top Die



Hot Spot in 3DIC Run



Elimination of Hot Spot After fixing HB Connection



Summary

- Multi-die (2.5D & 3D) Integrated Circuit systems require proper assessment of vulnerability to Electrostatic Discharge (ESD)
- To this end, novel modeling and simulation capabilities were utilized to analyze such a system
- Well-established ESD checks were applied to this system, involving assessing Current Density violations and point-to-point Resistance checks to the paths that traverse from a one die to another.

The outcome is that potential violations unique to the 3DIC system were identified, and whose identification is only possible through this unified simulation versus traditional standalone die simulations

Future tests will include assessing the paths through an interposer, and to compare violations that occur on standalone die simulations versus this effective multi-die system

ACKNOWLEDGEMENT

- I would like to sincerely thank the following people who helped in successful completion of this Study

Muhammad Zakir - Ansys
Kwangseok Choi - Ansys
Jaemyoung Choi - Ansys
Prabanjan Komari – Intel

Anila Azam

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